

This ALU take 2 inputs: A, B. A is 8-bit value fetch from external memory and B is 8-bit value from operand register. Sel is first four bits of 8-bit operation code of processor.

Flags are:	Zero	Carry	Sign	Parity
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B. Techniques to Achieve Low Power Design

Minimum Drive Strength, Efficient Mapping, Minimal LUT, BRAM, LVC MOS based Iostandard, LVDCI based Iostandard, Clock Gate and Power Gate are the current low power design techniques in VLSI circuit design. In this paper, we try to apply minimum drive strength on LVC MOS in our implementation of ALU in order to reduce power dissipation.

III. RESULTS

Below is top-level schematic of ALU, on which we experiment the effect of drive strength and IO standard in power consumption.

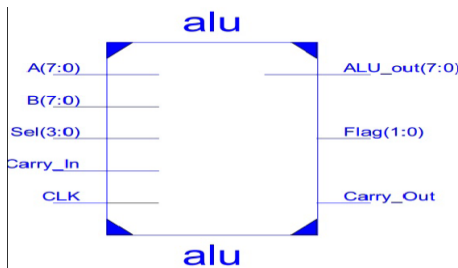


Figure. 3. Low Power ALU top level schematic

C. Dynamic Power is Proportional to Drive Strength

Dynamic power is a sum total of clock power, logic power, signal power and IO power. Clock power and Signal power is not affected by drive strength. Drive Strength mainly affect IOs Power that contribute in increase/decrease of Dynamic Power.

LVC MOS25 on 40nm Virtex-6 FPGA				
Drive Strength→	2mA	6mA	12mA	24mA
Clock Power	5mW	5mW	5mW	5mW
Signal Power	1mW	1mW	1mW	1mW
IOs Power	44mW	62mW	64mW	72mW
Dynamic Power	50mW	68mW	70mW	78mW
Leakage Power	1294mW	1294mW	1294mW	1294mW
Total Power	1344mW	1362mW	1364mW	1372mW

Here, if drive strength is 24mA, then dynamic power consumption of ALU is 78mW. In the same way, if drive strength is 2mA then the dynamic power consumption is 50mW. So, we observe that dynamic power is directly proportional to drive strength.

Here, if drive strength is 8mA, then dynamic power consumption of ALU is 26mW. In the same way, if drive strength is 2mA then the dynamic power consumption is 20mW. So, we observe that dynamic power is directly

proportional to drive strength. Migration from LVC MOS25 to LVC MOS12 reduces 2mW leakage power.

LVC MOS12 on 40nm Virtex-6 FPGA				
Drive Strength→	2mA	4mA	6mA	8mA
Clock Power	5mW	5mW	5mW	5mW
Signal Power	1mW	1mW	1mW	1mW
IOs Power	14mW	15mW	19mW	20mW
Dynamic Power	20mW	21mW	25mW	26mW
Leakage Power	1292mW	1292mW	1292mW	1292mW
Total Power	1312mW	1313mW	1317mW	1318mW

D. Dynamic Current is Proportional to Drive Strengt(DS)

Dynamic Current by LVC MOS25 on Virtex-6 FPGA					
Supply Summary		DS-2mA	DS-6mA	DS-16mA	DS-24mA
V _{ccint}	1.0 V	8mA	8mA	8mA	8mA
V _{ccaux}	2.5 V	0mA	1mA	1mA	2mA
V _{cc025}	1.2 V	16mA	23mA	24mA	26mA

According to above table, in LVC MOS25, dynamic current is directly proportional to drive strength. Dynamic current is maximum for 24mA drive strength and is lowest at 2mA drive strength. Current produced by V_{ccint} is not affected by drive strength. Only dynamic current produced by V_{ccaux} and V_{cc025} changes according to changes in drive strength.

Dynamic Current by LVC MOS12 on Virtex-6 FPGA				
Supply Summary		DS(2mA)	DS(6mA)	DS(8mA)
V _{ccint}	1.0 V	8mA	8mA	8mA
V _{ccaux}	2.5 V	0mA	1mA	1mA
V _{cc012}	1.2 V	10mA	12mA	14mA

According to above table, in LVC MOS12, dynamic current is directly proportional to drive strength. Dynamic current is maximum (i.e. 23mA) for 8mA drive strength and is lowest i.e. 18mA at 2mA drive strength. Current produced by V_{ccint} is not affected by drive strength. Only dynamic current produced by V_{ccaux} and V_{cc012} changes according to changes in drive strength.

LVC MOS on 40-nm FPGA			
V _{cco} →	LVC MOS12	LVC MOS18	LVC MOS25
	1.2V, DS=2	1.8V, DS=16	2.5V, DS=24
Clock Power	5mW	4mW	5mW
Signal Power	1mW	0mW	1mW
IOs Power	14mW	59mW	72mW
Dynamic Power	20mW	63mW	78mW
Total Power	1312mW	1359mW	1372mW

E. Different Low Voltage CMOS based on Voltage

Power dissipation depends on Iostandard. An input or output standard needs a specific Vcco voltage. We use the UCF file to select any LVCMOS standard that is compatible with the Vcco of the bank. Obviously the UCF file cannot supply a different voltage to the bank. Total Power is directly proportional to Vcco voltage. Power dissipation is highest at 2.5V and is lowest at 1.2V.

F. RTL Resource Estimation

PlanAhead provide resource estimation statistics based on the compiled RTL design. Here, RTL resource estimation has 73 out of 46560 LUT and 34 out of 240 IO on chip resource of Virtex-6 FPGA.

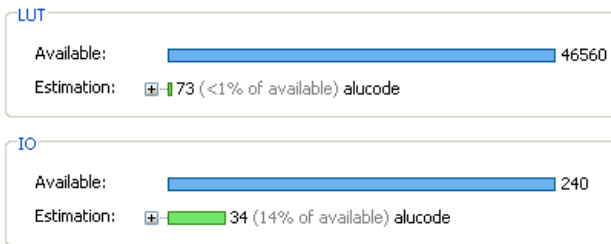


Figure 4. RTL resource statistics

G. Pre-Synthesis Power Estimation

Power estimation and analysis is gaining important as FPGAs increase in logic capacity and performance by migrating to 28-nm technology. Total power in an FPGA is the sum of two components: One is Static power and the other is Dynamic power. Using XCF, PCF, Virtex-6 Default operating condition and UCF timing constraint of 1000.0 MHz on clock net 'CLK' in power estimation, RTL dynamic power estimation is 41mw. Total power estimation on ALU is: 1044 mW.

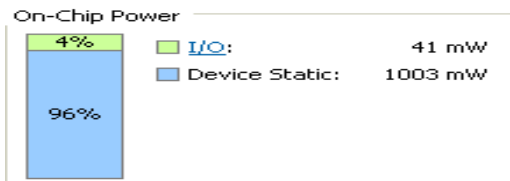


Figure 5. Pre-synthesis & Pre-implementation power consumption

H. Synthesis Estimation

In the process of converting a higher-level form of a design into a lower-level implementation of ALU, ISE uses Register, BUFG, LUT and IO as a on chip resource of FPGA.

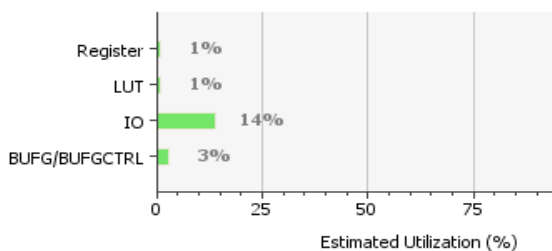


Figure 6. Post synthesis resource usage statistics

I. Netlist Estimation

Netlist usually convey connectivity information and provide nothing more than instances, nets, and perhaps some attributes. The netlist of ALU describes the connectivity of this design. It uses 1% Register, 1% LUT, 15% IO and 4% Global clock Buffer.

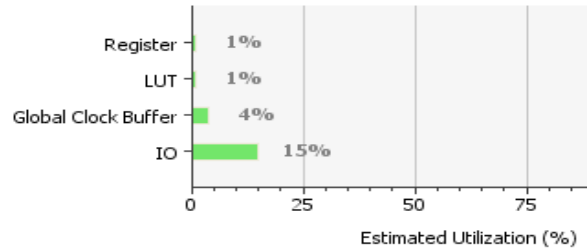


Figure 7. Low Power ALU Netlist Resource Usage Statistics

This net list has no demand for Block Memory, DSP48, Clock Manager, Tri-Mode Ethernet MAC, PCI Express, and Gigabit Transceiver.

J. Implemented Utilization

The summary of the device utilization after mapping and place and route of implementation phase are as following:

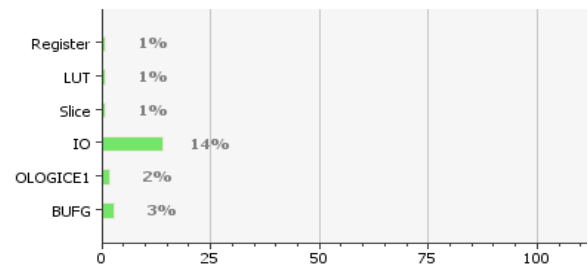


Figure 8. Post implementation of resource usage statistics of ALU

After mapping and place and routing, the device usage is the highest. It uses OLOGICE1 (Flip-flop packed into Output Logic) and Slice (elementary programmable logic block in Xilinx FPGAs) other than device utilized by netlist. This is using 1% register, 1% LUT, 1% slice, 14% IO, 2% output logic and 3% global clock buffer available in virtex-6 device family FPGA. Then, 1.523W dynamic power, 1.327W quiescent power and total 2.851W total power consumed.

	IO Standard on 40-nm FPGA		
	HSTL	DCI	LVCMOS25
Clock Power	7mW	7mW	5mW
Signal Power	0mW	0mW	1mW
IOs Power	168mW	433mW	72mW
Dynamic Power	175mW	450mW	78mW
Total Power	1470mW	1741mW	1372mW

K. LVC MOS in Compare to other IO Standard:

LVC MOS is more power efficient than any IO Standard use in this Virtex-6 FPGA. In view of power consumption, DCI is highest power consumer in between all used IO Standard in virtex-6 FPGA and LVC MOS is the best IO standard in term of power consumption.

IV. CONCLUSION

If LVC MOS25 is taken as IOSTANDARD, we saved 35.9% dynamic power and 36.11% dynamic power current by shifting drive strength from 24mA to 2mA. Migration from LVC MOS25 to LVC MOS12 reduces 2mW leakage power. If LVC MOS12 is taken as IOSTANDARD, we saved 30% dynamic power and 21.7% dynamic power current by shifting drive strength from 24mA to 2mA. LVC MOS is more power efficient than other IO standard likes HSTL or DCI supported in this Virtex-6 240T FPGA. In view of power consumption, DCI is highest power consumer and LVC MOS has the lowest power consumption. For any low power VLSI design, it is required to use LVC MOS as IO standard in ucf file.

V. FUTURE SCOPE

By migrating from iostandard LVC MOS to HSLVDCI or HSTL or HSTL_DCI or LVDCI or SSTL, we can explore new option to reduce dynamic power dissipation. Power dissipation is sure to vary with different iostandard and the logic behind that. This FPGA is Virtex-6 based on 40-nm technology. There is open area to explore this design in latest FPGA Virtex-7. Virtex-7 is based on 28-nm model technology which makes us capable to take the benefit of deeper sub micron circuit.

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